

Features

- Fast Read Access Time – 120 ns
- Fast Byte Write – 200 μ s
- Self-timed Byte Write Cycle
 - Internal Address and Data Latches
 - Internal Control Timer
 - Automatic Clear Before Write
- Direct Microprocessor Control
 - $\overline{\text{READY}}/\overline{\text{BUSY}}$ Open Drain Output
 - $\overline{\text{DATA}}$ Polling
- Low Power
 - 30 mA Active Current
 - 100 μ A CMOS Standby Current
- High Reliability
 - Endurance: 10^5 Cycles
 - Data Retention: 10 Years
- 5V $\pm$ 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-wide Pinout
- Industrial Temperature Ranges
- Green (Pb/Halide-Free) Packaging Option

1. Description

The AT28C64E is a low-power, high-performance 8,192 words by 8-bit nonvolatile electrically erasable and programmable read-only memory with popular, easy-to-use features. The device is manufactured with Atmel's reliable nonvolatile technology.

The AT28C64E is accessed like a Static RAM for the read or write cycles without the need for external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The device includes two methods for detecting the end of a write cycle, level detection of $\overline{\text{RDY}}/\overline{\text{BUSY}}$ (unless pin 1 is N.C.) and $\overline{\text{DATA}}$ Polling of I/O₇. Once the end of a write cycle has been detected, a new access for a read or write can begin.

The CMOS technology offers fast access times of 120 ns at low power dissipation. When the chip is deselected, the standby current is less than 100 μ A.

Atmel's AT28C64E has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32 bytes of EEPROM are available for device identification or tracking.



**64K (8K x 8)
Parallel
EEPROMs**

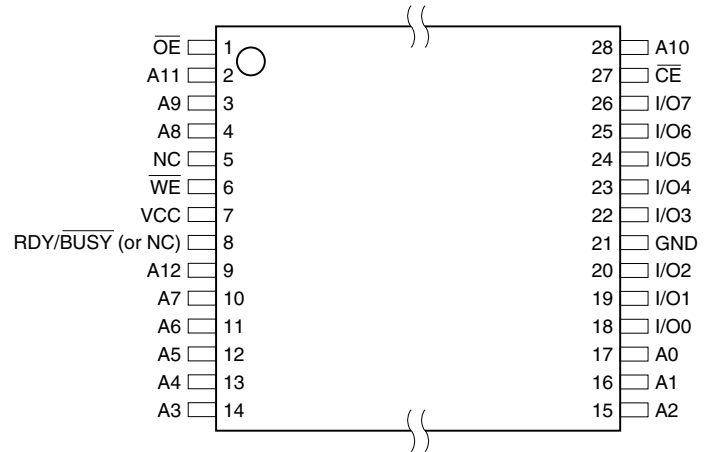
AT28C64E



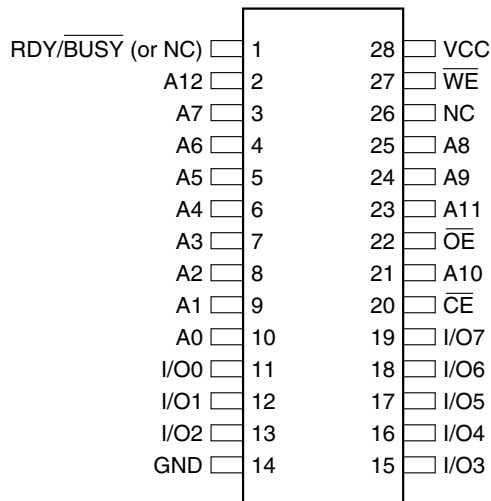
2. Pin Configurations

Pin Name	Function
A0 - A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/ $\overline{BUSY}$	Ready/Busy Output
NC	No Connect
DC	Don't Connect

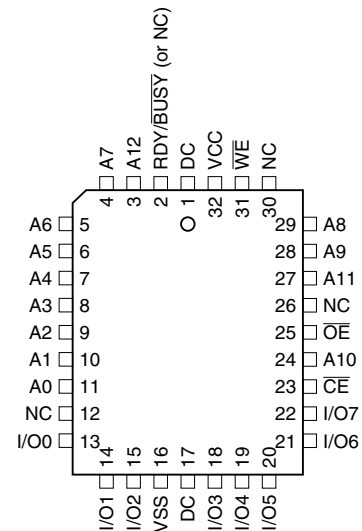
2.2 TSOP Top View



2.1 PDIP, SOIC Top View

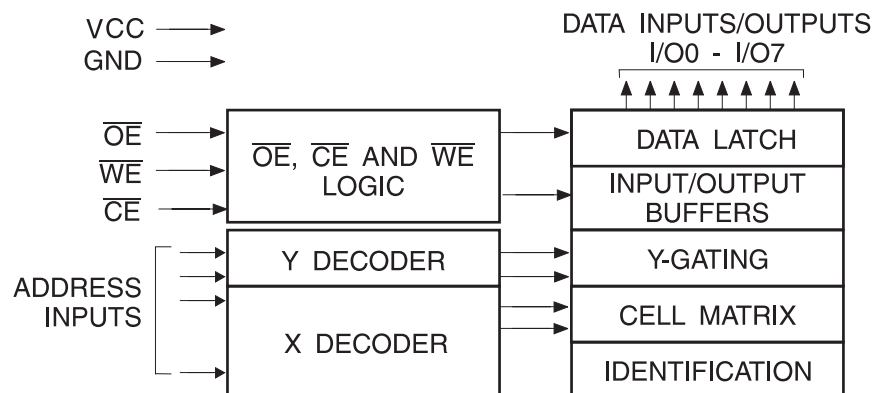


2.3 LCC, PLCC Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

3. Block Diagram



4. Absolute Maximum Ratings*

Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to $V_{CC} + 0.6V$
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

***NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

5. Device Operation

5.1 Read

The AT28C64E is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

5.2 Byte Write

Writing data into the AT28C64E is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC} , a read operation will effectively be a polling operation.

5.3 Fast Byte Write

The AT28C64E offers a byte write time of 200 μ s maximum. This feature allows the entire device to be rewritten in 1.6 seconds.

5.4 $\overline{RDY}/\overline{BUSY}$

Pin 1 is an open drain $\overline{RDY}/\overline{BUSY}$ output that can be used to detect the end of a write cycle. $\overline{RDY}/\overline{BUSY}$ is actively pulled low during the write cycle and is released at the completion of the write. The open-drain connection allows for OR-tying of several devices to the same $\overline{RDY}/\overline{BUSY}$ line.

5.5 $\overline{DATA}$ Polling

The AT28C64E provides $\overline{DATA}$ Polling to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

5.6 Write Protection

Inadvertent writes to the device are protected against in the following ways: (a) V_{CC} sense – if V_{CC} is below 3.8V (typical), the write function is inhibited; (b) V_{CC} power on delay – once V_{CC} has reached 3.8V, the device will automatically time out 5 ms (typical) before allowing a byte write; and (c) write inhibit – holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

5.7 Chip Clear

The contents of the entire memory of the AT28C64E may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

5.8 Device Identification

An extra 32 bytes of EEPROM memory are available to the user for device identification. By raising A_9 to 12 ± 0.5 V and using address locations 1FE0H to 1FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

6. DC and AC Operating Range

	AT28C64E-12
Operating Temperature (Case)	-40°C - 85°C
V _{CC} Power Supply	5V ±10%

7. Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V _{IL}	V _{IL}	V _{IH}	D _{OUT}
Write ⁽²⁾	V _{IL}	V _{IH}	V _{IL}	D _{IN}
Standby/Write Inhibit	V _{IH}	X ⁽¹⁾	X	High Z
Write Inhibit	X	X	V _{IH}	
Write Inhibit	X	V _{IL}	X	
Output Disable	X	V _{IH}	X	High Z
Chip Erase	V _{IL}	V _H ⁽³⁾	V _{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
 2. Refer to AC programming waveforms.
 3. V_H = 12.0V ±0.5V.

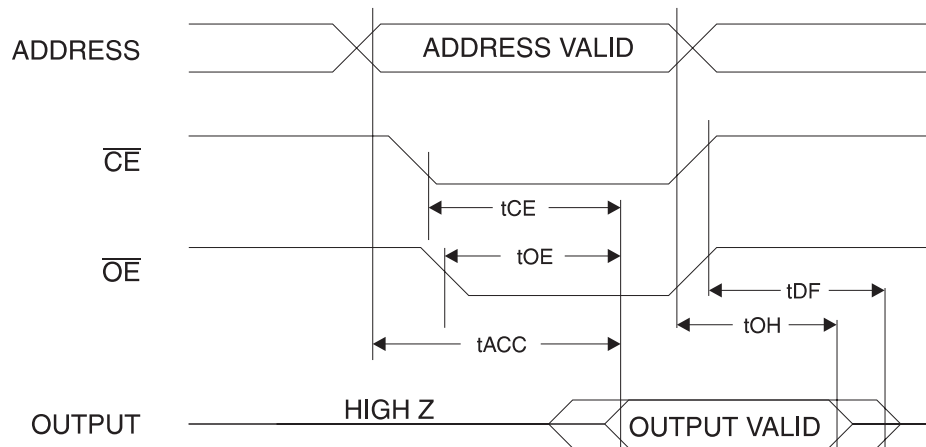
8. DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I _{LI}	Input Load Current	V _{IN} = 0V to V _{CC} + 1V		10	μA
I _{LO}	Output Leakage Current	V _{I/O} = 0V to V _{CC}		10	μA
I _{SB1}	V _{CC} Standby Current CMOS	$\overline{CE} = V_{CC} - 0.3V$ to V _{CC} + 1.0V		100	μA
I _{SB2}	V _{CC} Standby Current TTL	$\overline{CE} = 2.0V$ to V _{CC} + 1.0V		3	mA
I _{CC}	V _{CC} Active Current AC	f = 5 MHz; I _{OUT} = 0 mA $\overline{CE} = V_{IL}$		45	mA
V _{IL}	Input Low Voltage			0.8	V
V _{IH}	Input High Voltage		2.0		V
V _{OL}	Output Low Voltage	I _{OL} = 2.1 mA = 4.0 mA for RDY/ $\overline{BUSY}$		0.45	V
V _{OH}	Output High Voltage	I _{OH} = -400 μA	2.4		V

9. AC Read Characteristics

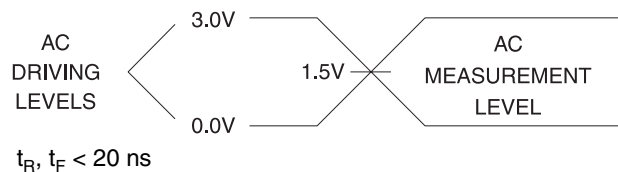
Symbol	Parameter	AT28C64E-12		Units
		Min	Max	
t_{ACC}	Address to Output Delay		120	ns
$t_{CE}^{(1)}$	$\overline{CE}$ to Output Delay		120	ns
$t_{OE}^{(2)}$	$\overline{OE}$ to Output Delay	10	60	ns
$t_{DF}^{(3)(4)}$	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	45	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		ns

10. AC Read Waveforms⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

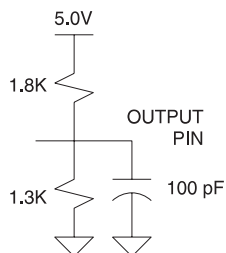


- Notes:
- $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC} .
 - $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC} .
 - t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first ($C_L = 5$ pF).
 - This parameter is characterized and is not 100% tested.

11. Input Test Waveforms and Measurement Level



12. Output Test Load



13. Pin Capacitance

$f = 1 \text{ MHz}$, $T = 25^\circ\text{C}$ ⁽¹⁾

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	$V_{IN} = 0V$
C_{OUT}	8	12	pF	$V_{OUT} = 0V$

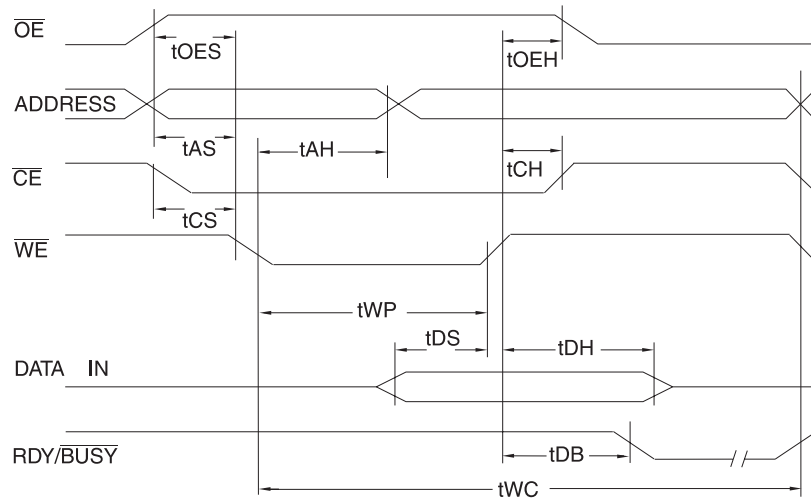
Note: 1. This parameter is characterized and is not 100% tested.

14. AC Write Characteristics

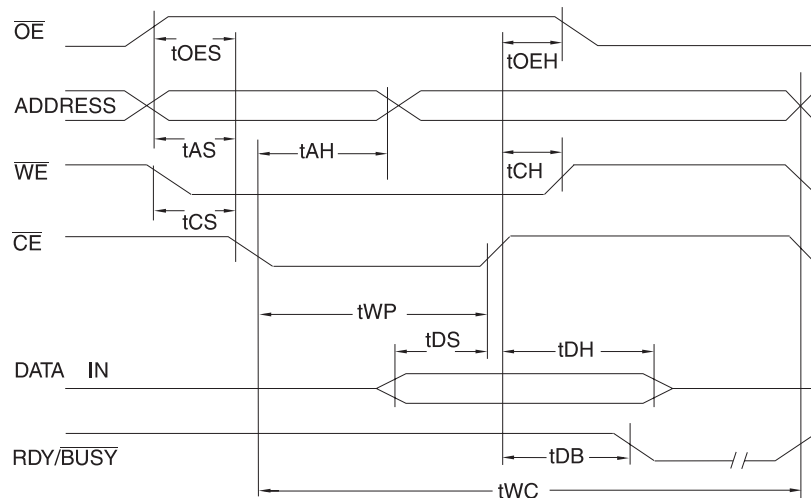
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Setup Time	10		ns
t_{AH}	Address Hold Time	50		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100	1000	ns
t_{DS}	Data Setup Time	50		ns
$t_{DH}, t_{OE H}$	Data, $\overline{OE}$ Hold Time	10		ns
t_{CS}, t_{CH}	$\overline{CE}$ to $\overline{WE}$ and $\overline{WE}$ to $\overline{CE}$ Setup and Hold Time	0		ns
t_{DB}	Time to Device Busy		50	ns
t_{WC}	Write Cycle Time		200	μ s

15. AC Write Waveforms

15.1 $\overline{WE}$ Controlled



15.2 $\overline{CE}$ Controlled

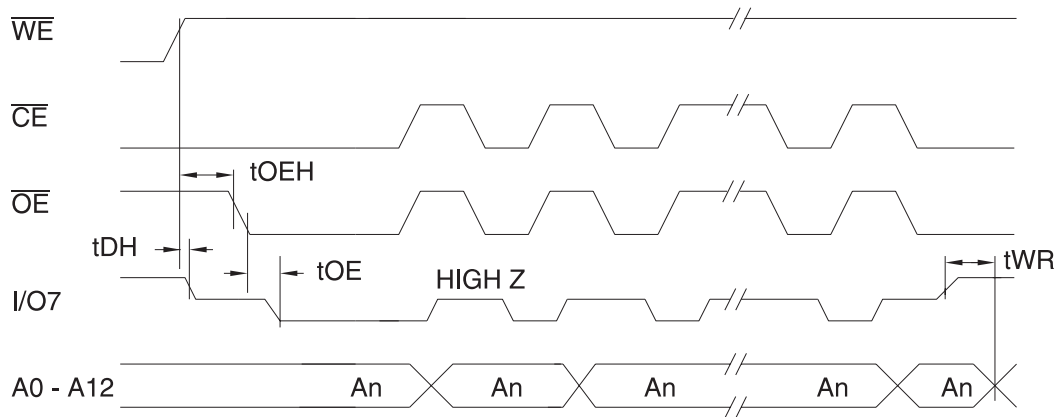


16. Data Polling Characteristics⁽¹⁾

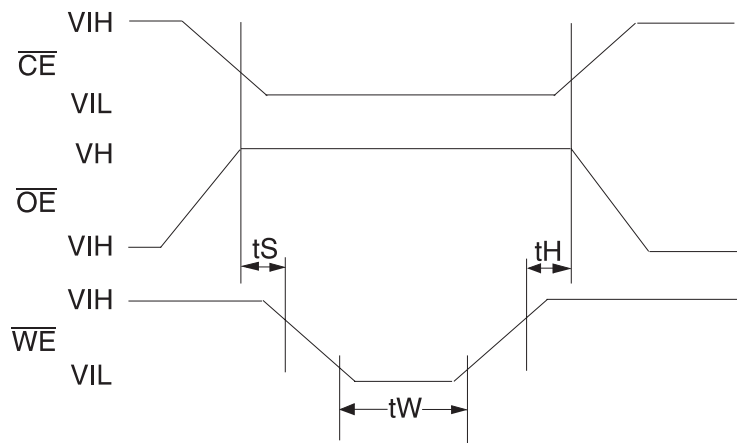
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
$t_{OE\overline{H}}$	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay ⁽²⁾				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See "AC Read Characteristics".

17. Data Polling Waveforms

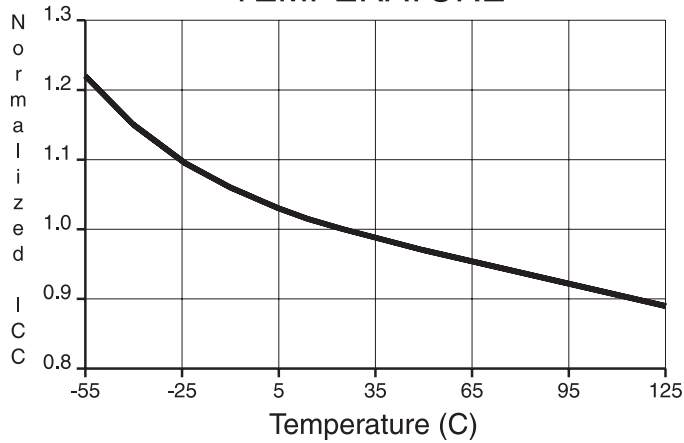


18. Chip Erase Waveforms

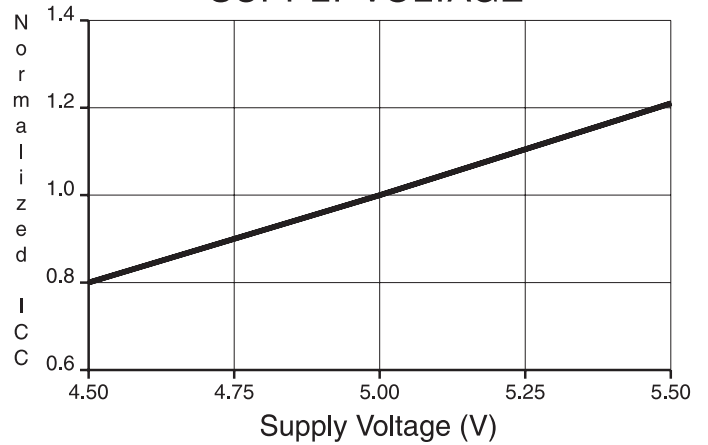


$t_S = t_H = 1 \mu\text{sec (min.)}$
 $t_W = 10 \text{ msec (min.)}$
 $V_H = 12.0 \pm 0.5V$

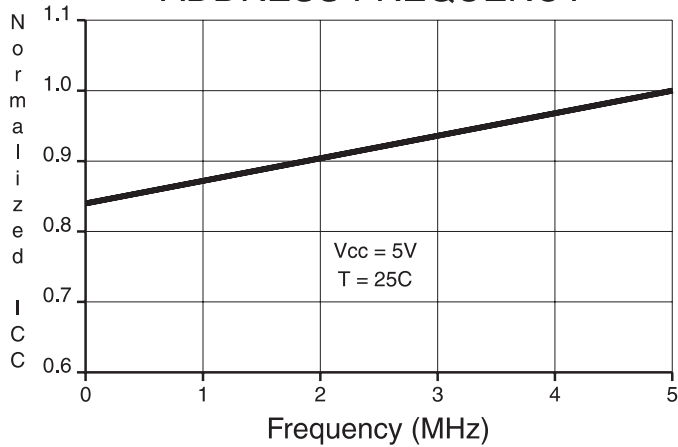
NORMALIZED SUPPLY CURRENT vs.
TEMPERATURE



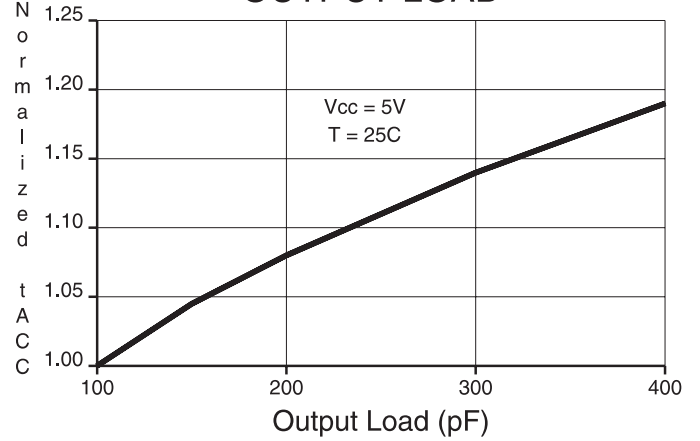
NORMALIZED SUPPLY CURRENT vs.
SUPPLY VOLTAGE



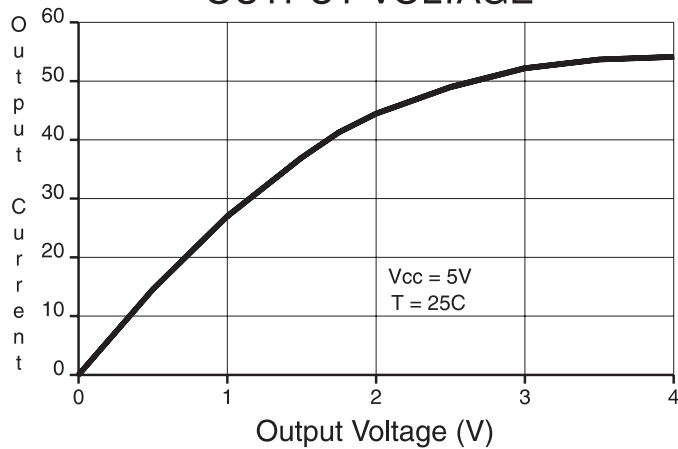
NORMALIZED SUPPLY CURRENT vs.
ADDRESS FREQUENCY



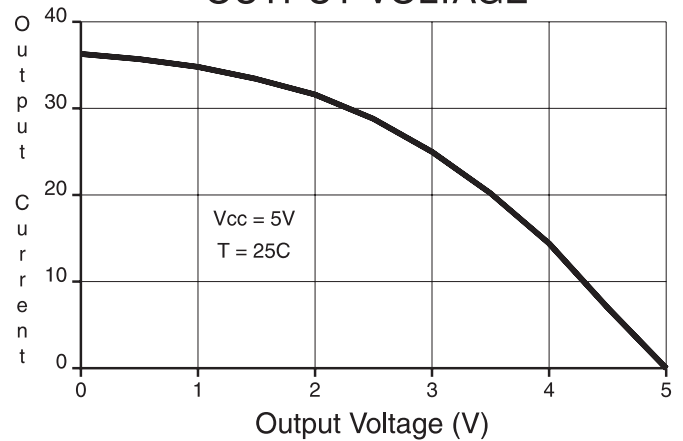
NORMALIZED ACCESS TIME vs.
OUTPUT LOAD



OUTPUT SINK CURRENT vs.
OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs.
OUTPUT VOLTAGE



19. Ordering Information

19.1 Standard Package

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	45	0.1	AT28C64E-12JI AT28C64E-12PI AT28C64E-12SI AT28C64E-12TI	32J 28P6 28S 28T	Industrial (-40° C to 85° C)

19.2 Green Package (Pb/Halide-free)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	45	0.1	AT28C64E-12JU AT28C64E-12PU AT28C64E-12SU AT28C64E-12TU	32J 28P6 28S 28T	Industrial (-40° C to 85° C)

19.3 Package Type

Package Type	Description
32J	32-lead, Plastic J-leaded Chip Carrier (PLCC)
28P6	28-lead, 0.600" Wide, Plastic Dull Inline Package (PDIP)
28S	28-lead, 0.300" Wide, Plastic Gull Wing, Small Outline (SOIC)
28T	28-lead, Plastic Thin Small Outline Package (TSOP)

20. Valid Part Numbers

The following table lists standard Atmel® products that can be ordered.

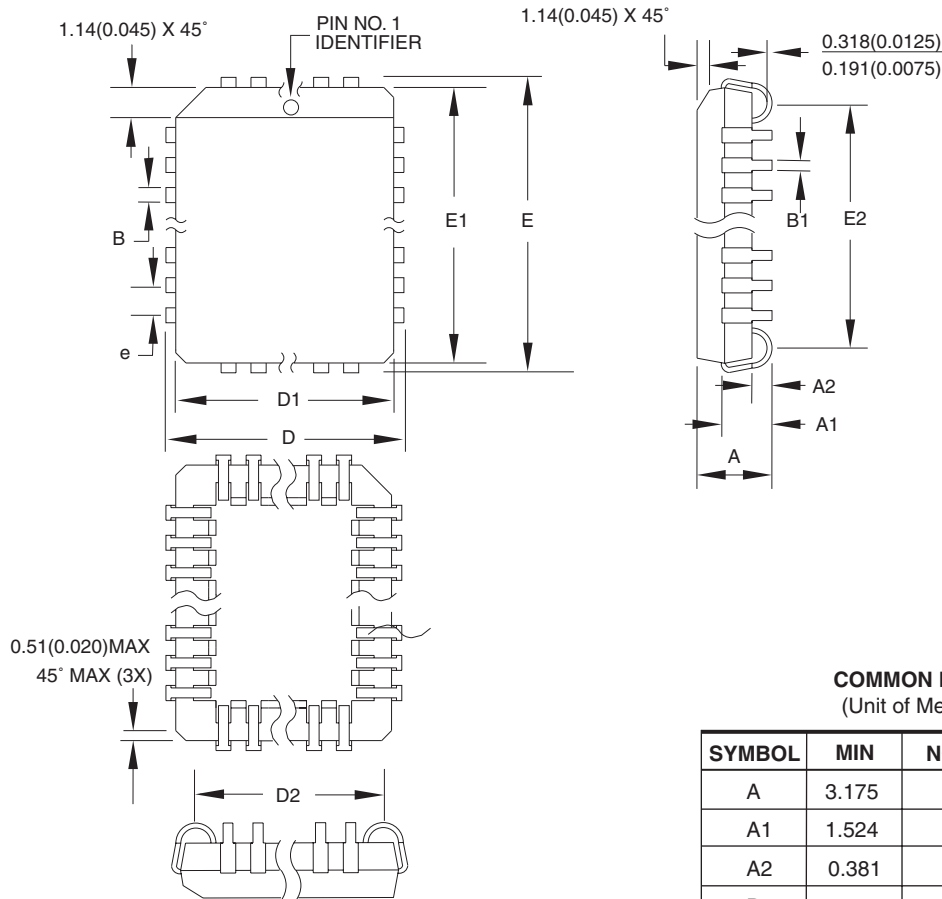
Device Numbers	Speed	Package and Temperature Combinations
AT28C64E	12	JI, JU, PI, PU, SI, SU, TI, TU

21. Die Products

Reference Section: Parallel EEPROM Die Products

22. Packaging Information

22.1 32J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	3.175	–	3.556	
A1	1.524	–	2.413	
A2	0.381	–	–	
D	12.319	–	12.573	
D1	11.354	–	11.506	Note 2
D2	9.906	–	10.922	
E	14.859	–	15.113	
E1	13.894	–	14.046	Note 2
E2	12.471	–	13.487	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-016, Variation AE.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
 3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE

32J, 32-lead, Plastic J-leaded Chip Carrier (PLCC)

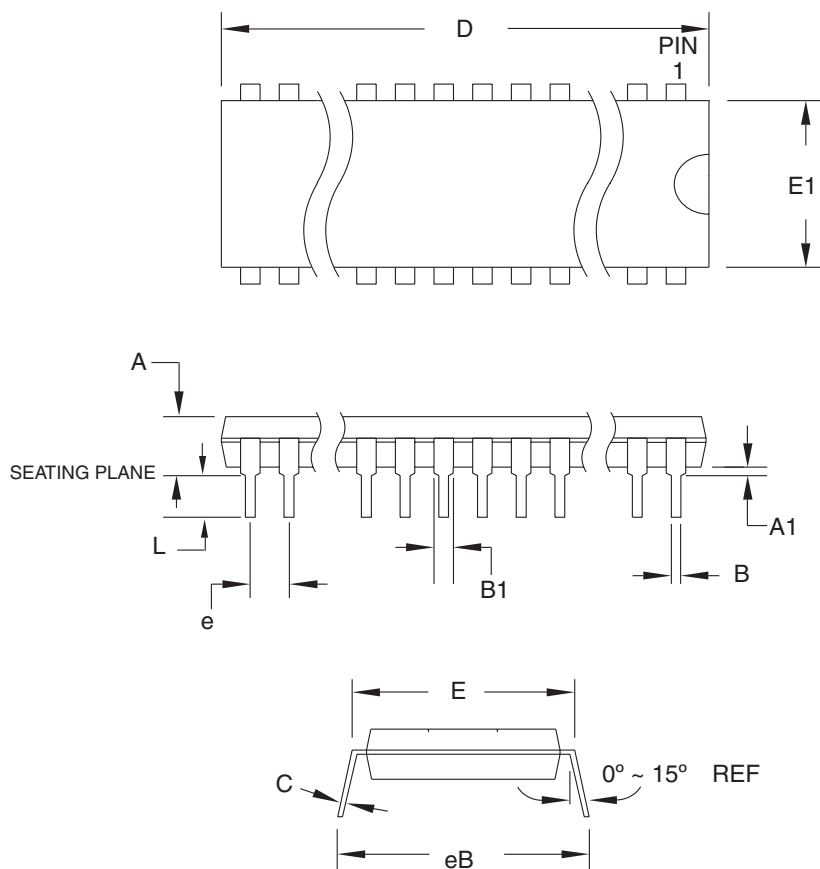
DRAWING NO.

32J

REV.

B

22.2 28P6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	4.826	
A1	0.381	—	—	
D	36.703	—	37.338	Note 2
E	15.240	—	15.875	
E1	13.462	—	13.970	Note 2
B	0.356	—	0.559	
B1	1.041	—	1.651	
L	3.048	—	3.556	
C	0.203	—	0.381	
eB	15.494	—	17.526	
e	2.540 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-011, Variation AB.
 2. Dimensions D and E1 do not include mold Flash or Protrusion.
Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE

28P6, 28-lead (0.600"/15.24 mm Wide) Plastic Dual
Inline Package (PDIP)

DRAWING NO.

28P6

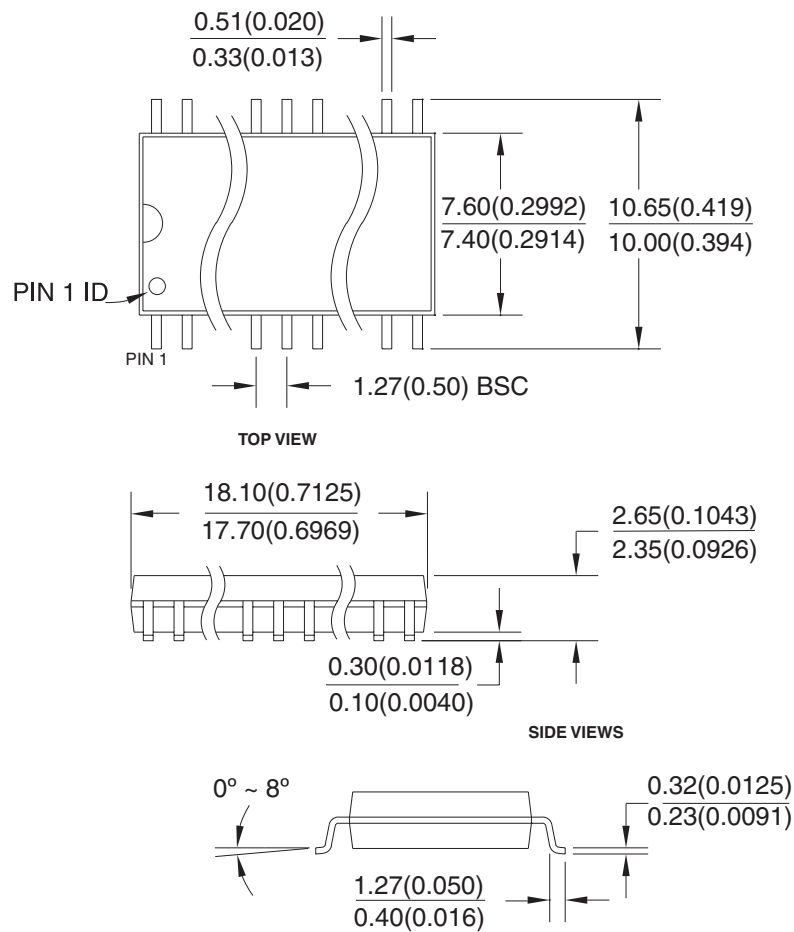
REV.

B



22.3 28S – SOIC

Dimensions in Millimeters and (Inches).
Controlling dimension: Millimeters.



8/4/03



2325 Orchard Parkway
San Jose, CA 95131

TITLE

28S, 28-lead, 0.300" Body, Plastic Gull Wing Small Outline (SOIC)
JEDEC Standard MS-013

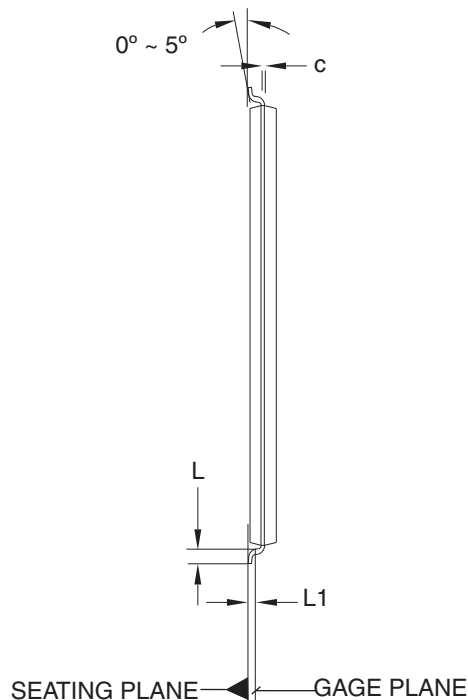
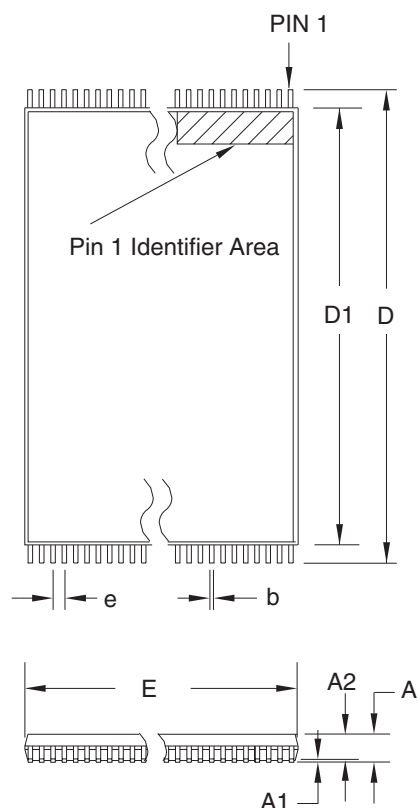
DRAWING NO.

28S

REV.

B

22.4 28T – TSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	1.20	
A1	0.05	—	0.15	
A2	0.90	1.00	1.05	
D	13.20	13.40	13.60	
D1	11.70	11.80	11.90	Note 2
E	7.90	8.00	8.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	—	0.21	
e	0.55 BASIC			

- Notes:
1. This package conforms to JEDEC reference MO-183.
 2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
 3. Lead coplanarity is 0.10 mm maximum.

12/06/02



2325 Orchard Parkway
San Jose, CA 95131

TITLE

28T, 28-lead (8 x 13.4 mm) Plastic Thin Small Outline
Package, Type I (TSOP)

DRAWING NO.

28T

REV.

C





Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe

Atmel Sarl
Route des Arsenalux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

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00011-PEEPR-10/06